Application No. 10/824,594
Attorney Docket: ND-448US (HAR.024)

REMARKS

Claims 1-19 are all the claims presently pending in the application. Claim 8 has been amended to more particularly define the invention. Claims 10-19 have been added to assure Applicant the degree of protection to which his invention entitles him.

It is noted that the claim amendments are made only to assure grammatical and idiomatic English and improved form under United States practice, and are not made to distinguish the invention over the prior art or narrow the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 1-9 stand rejected under 35 U.S.C. §102(e) as being anticipated by Bartels et al. (U.S. Patent Application Publication No. US 2003/0208704).

This rejection is respectfully traversed in the following discussion.

THE CLAIMED INVENTION

The claimed invention is directed to an information processing apparatus. A first and second processing means perform the same process in synchronism with each other. Adjustment means adjust orders of output data from the first and second information processing means so as to correspond to each other to discriminate whether or not the output data coincide with each other. A re-construction means re-constructs a plurality of output data of the second information processing means, based on a plurality of output data of the first information processing means. A comparison means compares the output data of the

first information processing means and the output data of the second information processing means with each other.

The information processing apparatus can thus discriminate, even when the orders of output data of a plurality of CPU modules differ from each other, whether or not the operations of the CPU modules coincide with each other.

In a conventional information processing apparatus for use with a fault-tolerant system, even if each of the plurality of processors normally operates, an interruption timing for interruption handling of one of the processors sometimes displaces output of one processor from that of the other processor, thereby making the timings or the orders of output data of the processors different. If the order of the output data of one of the processors changes, then the output data of the processors become different from each other at a certain point of time. Therefore, the lack of coincidence of the output data of the processors is detected in error, as described on pages 1-2 of the specification.

The claimed invention, on the other hand, provides an information processing apparatus which can discriminate, even if the orders of output data differ from each other or if any of output data is interrupted, whether or not the operations of the CPU modules coincide with each other.

THE PRIOR ART REJECTIONS

The Bartels Reference

The Examiner alleges that Bartels teaches the claimed invention. Applicant submits, however, that there are elements of the claimed invention, which are neither taught nor

suggested by Bartels.

Bartels discloses a system for a computing platform to detect and correct multi-bit data failures in data. Bartels discloses parallel processing lanes in a lockstep architecture.

With regard to independent claim 1, Bartels fails to disclose "adjustment means for adjusting orders of output data from first and second information processing means." Instead, Bartels has no reason to adjust orders of output data. Bartels discloses error detection and correction (EDC) components 116 and 118, which use the error detection and correction block to detect and correct single-bit faults within each stored data word in memory. That is, the EDC components function to check the integrity of the *storage* of the data. See Bartels para. [12]-[15], [20], [29], [30]. Bartels discloses a bit-by-bit comparison of the redundant memory arrays' contents. However, Bartels discloses the parallel processing lanes operating only in lockstep and does not address the situation of the data output of the processors being correctly computed but asynchronous (i.e., out of lockstep) such that a bit-by-bit comparison would indicate a discrepancy between such correct data outputs. Bartels also fails to disclose adjusting the orders of output data.

Hence, turning to the clear language of the claims, in Bartels there is no teaching or suggestion of "adjustment means for adjusting orders of output data from said first and second information processing means so as to correspond to each other," as required by independent claim 1. The remaining independent claims have similar language.

With regard to dependant claim 2 which depends from and inherits all features of independent claim 1, Bartels fails to disclose each element of independent claim 1 as discussed above.

With regard to dependant claim 3 which depends from and inherits all features of dependent claim 2, Bartels fails to disclose each element of dependent claim 2 as discussed above. Bartels further fails to disclose wherein said adjustment means compares the output data of said first and second information processing means "when an amount of output data stored in any one of said first and second storage means reaches a predetermined amount." Bartels discloses the parallel processing lanes operating only in lockstep and is not concerned with the amount of output data in the first or second storage means reaching a predetermined amount.

Hence, turning to the clear language of the claims, in Bartels there is no teaching or suggestion of "said adjustment means compares, when the amount of output data stored in any one of said first and second storage means reaches a predetermined amount, the output data of said first information processing means stored in said first storage means and the output data of said second information processing means stored in said second storage means with each other with the output data adjusted in order so as to correspond to each other," as required by claim 3.

With regard to dependant claim 4 which depends from and inherits all features of dependent claim 2, Bartels fails to disclose each element of dependent claim 2 as discussed above. Bartels further fails to disclose wherein said adjustment means further includes designation means for "designating a frequency with which the discrimination is to be performed to a frequency lower than a frequency with which the output data of the first and second information processing means are received." Instead, Bartels discloses that the bit-by-bit comparison of the redundant memory arrays' contents is performed after the EDC

components process and correct single-bit faults within a data word. Bartels, para. [29].

Hence, turning to the clear language of the claims, in Bartels there is no teaching or suggestion of "said adjustment means further includes designation means for designating the frequency with which the discrimination is to be performed to a frequency lower than a frequency with which the output data of said first and second information processing means are received," as required by claim 4.

With regard to independent claim 5, Bartels fails to disclose "adjustment means including reconstruction means for re-constructing a plurality of output data of said second information processing means." Instead, Bartels discloses a means to correct stored data which has been determined to have become faulty or corrupted by overwriting with a fault-free copy of the data. Bartels, para. [15], [30]-[32]. Bartels is silent on any rearrangement of fault-free data in the storage means.

Hence, turning to the clear language of the claims, in Bartels there is no teaching or suggestion of "adjustment means including re-construction means for re-constructing a plurality of output data of said second information processing means based on a plurality of output data of said first information processing means," as required by claim 5.

With regard to dependant claim 6 which depends from and inherits all features of independent claim 5, Bartels fails to disclose each element of independent claim 5 as discussed above. Further, and as discussed with regard to claim 1 above, Bartels fails to disclose "changing an order of the output data of the second information processing means stored in the second storage means based on the order of the output data of the first information processing means stored in the first storage means."

Hence, turning to the clear language of the claims, in Bartels there is no teaching or suggestion of "said re-construction means changes an order of the output data of said second information processing means stored in said second storage means," as required by claim 6.

With regard to dependant claim 7 which depends from and inherits all features of independent claim 5, Bartels fails to disclose each element of independent claim 5 as discussed above. Further, Bartels fails to disclose dividing and re-coupling the output data of the second information processing means stored in the second storage means based on the output data of the first information processing means stored in the first storage means. As discussed with regard to claim 5 above, Bartels discloses correcting corrupted or faulty data but is silent on any rearrangement of fault-free data in the storage means.

Hence, turning to the clear language of the claims, in Bartels there is no teaching or suggestion of "said re-construction means divides and re-couples the output data," as required by claim 7.

With regard to independent claim 8, Bartels fails to disclose "adjustment means for selecting one of data of a plurality of data of a second output of said second information processing means which data is determined to correspond to one of data of a plurality of data of a first output of said first information processing means." As discussed with regard to independent claim 1 above, Bartels discloses parallel processing lanes operating only in lockstep. Bartels discloses that data is retrieved from the memory arrays; Bartels fails to disclose any ability to discriminate among or select a data from a plurality of data outputs.

Hence, turning to the clear language of the claims, in Bartels there is no teaching or suggestion of "adjustment means for selecting one of data of a plurality of data of a second

output of said second information processing means which data is determined to correspond to one of data of a plurality of data of a first output of said first information processing means," as required by claim 8.

With regard to dependant claim 9 which depends from and inherits all features of independent claim 8, Bartels fails to disclose each element of independent claim 8 as discussed above. Bartels further fails to disclose wherein "said adjustment means searches the second storage means for one of the data of the second output corresponding to one of the data output of the first output of the first information processing means stored in the first storage means." Bartels discloses the parallel processing lanes operating only in lockstep and is silent on the case of the data of the second output of the second information processing means not being synchronous with the data of the first output of the first information processing means. Bartels discloses a bit-by-bit comparison of the independent memory arrays' contents and would generate an interrupt when the bit-by-bit comparison fails, as would happen when the data from the first output from the first information processing means in the first storage means and the corresponding data from the second output of the second information processing means in the second storage means are not received synchronously.

Hence, turning to the clear language of the claims, in Bartels there is no teaching or suggestion of "said adjustment means searches said second storage means for one of the data of the second output corresponding to one of the data of the first output of said first information processing means stored in said first storage means," as required by claim 9.

Therefore, Applicant submits that there are elements of the claimed invention that are

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not taught or suggest by Bartels. Therefore, the Examiner is respectfully requested to withdraw this rejection.

CONCLUSION

In view of the foregoing, Applicant submits that claims 1-19, all the claims presently pending in the application, are patentably distinct over the prior art of record and are allowable, and that the application is in condition for allowance. Such action would be appreciated.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned attorney at the local telephone number listed below to discuss any other changes deemed necessary for allowance in a telephonic or personal interview.

To the extent necessary, Applicant petitions for an extension of time under 37 CFR §1.136. The Commissioner is authorized to charge any deficiency in fees, including extension of time fees, or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 3 January 2007

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CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that I am filing this Response by facsimile with the United States Patent and Trademark Office to Examiner Truong, Loan, Group Art Unit 2114 at fax number (571) 273-8300 this 3rd day of January 2007.

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